Notice of Allowability	Application No.	Applicant(s)	
	10/777,207	FISCHER ET AL.	
	Examiner	Art Unit	
	PHUC T. DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on November 28, 2005*.

2. ☒ The allowed claim(s) is/are *1-3, 5 and 8-11 (renumbered as in new claims 1-8)*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

PHUC T DANG
Primary Examiner
Art Unit: 2818

Figures 4a-c show fabrication steps of a semiconductor device in accordance with a second embodiment of the present invention.

Figure 5 shows a semiconductor device in accordance with a third embodiment of the present invention.

Figures 6a,6b show fabrication steps of a semiconductor device in accordance with a fourth embodiment of the present invention.

Figure 7 shows a semiconductor device in accordance with a fifth embodiment of the present invention.

Figure 8 shows a semiconductor device in accordance with a sixth embodiment of the present invention

In the figures, identical reference symbols designate identical or functionally identical constituent parts.

DETAILED DESCRIPTION OF THE INVENTION

Figures 1a, 1b are a diagrammatic illustration of a semiconductor device in accordance with a first embodiment of the present invention.

Accurately setting the threshold voltage of field-effect transistors is a necessity for a whole host of circuit concepts. In this case, varying the gate capacitance, altering the substrate doping or else influencing the flat-band voltage have been employed as hardware possibilities. In this case, the ratio of the root of the substrate doping to the gate

In accordance with a further preferred embodiment, the first doping region and the second doping region are provided at the surface of a semiconductor substrate and are isolated by an isolation trench filled with an insulator material, the gate structure being provided at least on the trench bottom.

In accordance with a further preferred embodiment, the gate structure is provided on the trench bottom and the trench walls.

In accordance with a further preferred embodiment, the isolation trench has a greater depth extent in the semiconductor substrate than the first doping region and the second doping region.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the description below.

In the figures:

Figures 1a,/b	show a semiconductor device in accordance with a first embodiment of the present invention.
Figure 2	shows a flat-band voltage on the thickness of the first gate insulation layer in the first embodiment of the present invention.
Figure 3	shows a known semiconductor device in the form of a memory cell with a selection transistor and a trench capacitor with an insulation collar.